**IN THE CLAIMS:**

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND the claims in accordance with the following:

1. (CURRENTLY AMENDED) An information-processing device that executes a specific process more frequently than other processes among a variety of processes, said information-processing device comprising:

a first processor, having a single program counter, configured as hardware implementation to execute an ~~entire~~ instruction set corresponding to the variety of processes; and

a second processor configured as hardware implementation to execute a portion or entirety of the same instruction set that the first processor executes, said second processor including a plurality of program counters for executing a plurality of processes simultaneously so as to execute a part of said instruction set corresponding to the specific process more efficiently than said first processor,

wherein the specific process is assigned to said second processor ~~executes the specific process~~ for execution by the second processor whereas the other processes are assigned to said first processor ~~executes the other processes~~ for execution by the first processor, and each process is comprised of a series of instructions, the first processor and the second processor being configured such that a series of instructions executed by the first processor is separate from and independent of a series of instructions executed by the second processor.

2. (Previously Presented) The information-processing device as claimed in claim 1, wherein all the processes are allocated to said second processor initially, wherein said second processor passes a given process to said first processor by interrupting said first processor in a case in which an instruction other than the part of the instruction set corresponding to the specific process must be executed.

3. (Previously Presented) The information-processing device as claimed in claim 1, wherein all the processes are allocated to said second processor initially, wherein said second

processor passes a given process to said first processor by interrupting said first processor when an instruction that cannot be executed or cannot be efficiently executed by said second processor appears in said given process.

4. (Previously Presented) The information-processing device as claimed in claim 3, wherein said instruction that cannot be executed or cannot be efficiently executed by said second processor is a floating-point arithmetic operation.

5. (Previously Presented) The information-processing device as claimed in claim 1, wherein said second processor is capable of executing the part of said instruction set corresponding to the specific process more efficiently than said first processor by executing said specific process in parallel by use of at least one of a multi-threading method and a multi-processing method.

6. (Previously Presented) The information-processing device as claimed in claim 1, wherein said first processor is a general-purpose processor, wherein said second processor is a transaction processor designed to efficiently execute a transaction process as the specific process.

7. (Previously Presented) The information-processing device as claimed in claim 1, wherein said first processor and said second processor share a memory space.

8. (Previously Presented) The information-processing device as claimed in claim 1, wherein said information-processing device includes a plurality of first processors and second processors.

9. (CURRENTLY AMENDED) An information-processing device that executes a specific process more frequently than other processes among a variety of processes, said information-processing device comprising:

a first processor, having a single program counter, configured as hardware implementation to execute an ~~entire~~ instruction set and designed to execute variety of processes; and

a second processor configured as hardware implementation to execute a portion or entirety of the same instruction set that ~~the~~ said ~~second~~ first processor executes, said second processor including a plurality of program counters for executing multiples of specific ~~the variety of~~ processes concurrently so as to achieve more efficient execution than said first processor,

wherein the specific process is assigned to said second processor ~~executes the specific process~~ for execution by the second processor whereas the other processes are assigned to said first processor ~~executes the other processes~~ for execution by the first processor, and each process is comprised of a series of instructions, the first processor and the second processor being configured such that a series of instructions executed by the first processor is separate from and independent of a series of instructions executed by the second processor.

10. (Previously Presented) The information-processing device as claimed in claim 9, wherein all the processes are allocated to said second processor initially, wherein said second processor passes a given process to said first processor in a case in which an instruction other than the part of the instruction set corresponding to the specific process must be executed.

11. (Previously Presented) The information-processing device as claimed in claim 9, wherein all the processes are allocated to said second processor initially, wherein said second processor passes a given process to said first processor when an instruction that cannot be executed appears or the execution of the process is judged not efficient by said second processor in said given process.

12. (Previously Presented) The information-processing device as claimed in claim 11, wherein said instruction that cannot be executed or cannot be efficiently executed by said second processor is a floating-point arithmetic operation.

13. (Previously Presented) The information-processing device as claimed in claim 9, wherein said second processor is capable of executing all or the part of said instruction set corresponding to the specific process more efficiently than said first processor by executing said specific processes in parallel by use of at least one of a multi-threading method and a multi-processing method.

14. (Previously Presented) The information-processing device as claimed in claim 9, wherein said first processor is a general-purpose processor, wherein said second processor is a transaction processor designed to efficiently execute a transaction process as the specific process.

15. (Previously Presented) The information-processing device as claimed in claim 9, wherein said first processor and said second processor share common memory address space.

16. (Previously Presented) The information-processing device as claimed in claim 9, wherein said information-processing device includes a plurality of first processors and second processors.

17. (Cancelled)

18. (Cancelled)

19. (Cancelled)